A novel rearrangeable non-blocking architecture for 2D MEMS optical space switches

ABSTRACT
The tremendous growth of digital communications and the rapid rise of all-optical networks require flexible and reliable means of network management. Optical switches are key components in such a network which provide a flexible platform for data traffic routing. They also improve network survivability under faults. MEMS-based optical switches, incorporating a new promising optical switch technology, have been getting increased attention recently. In this paper, we propose a new rearrangeable non-blocking architecture for 2D MEMS optical space switches. A simple routing/mirror control algorithm is given to guarantee the new architecture to be rearrangeable non-blocking in nature. By comparing with the lower bound obtained for the number of micro-mirrors in a general rearrangeable non-blocking 2D MEMS switches, the proposed architecture is found to be an optimal one.

Gangxiang Shen
Tee Hiang Cheng
Chao Lu
Teck Yoong Chai
Network Technology Research Center
Nanyang Technological University
Singapore

Sanjay K. Bose
Department of Electrical Engineering
Indian Institute of Technology, Kanpur
Kanpur, India

1 Introduction

The tremendous growth of digital communications and the rapid rise of dense wavelength division multiplexing (DWDM) technology [1-4] have generated a demand for more flexible and reliable means of network management. The capabilities of optimising, routing, protecting and restoring light-paths in a real-time fashion will be critical issues in the management and operation of all optical networks. Optical switches at the optical cross-connect (OXC) nodes will be the crucial fibre-optic components to seamlessly maintain network survivability and will also provide a flexible platform for light-path operation [5-7]. By controlling these switches appropriately, one can provision and release light-paths between node pairs on demand. Moreover, network failures may be handled by quickly rerouting the affected lightpaths by rerouting them through alternate routes [8-10]. Such a network will also support high data throughputs and will provide full protocol transparency.

Based on the different kinds of fabrication technologies used, we may divide optical switches into several categories [11-13]. These include optomechanical switches, wave-guide solid-state switches [14-19], liquid-crystal optical switches [20-21], micro-electromechanical (MEMS) optical switches [22-25], and bubble optical switches [26-28]. Optomechanical switches are widely employed in traditional applications. They have the characteristics of good performance and low cost, but have large size, large element mass and slow switching times. Waveguide-based solid-state switches could be in the form of electro-optical switches [14-15], thermal-optical switches [16-17] or acousto-optical switches [18-19]. These switches share the common characteristic of having fast switching times, but their disadvantages are high cost, poor crosstalk and high insertion loss. Liquid-crystal optical switches are potential low-cost optical switches [20]. Their technology enables multiple-channel switches to be fabricated, but the disadvantages are high loss, considerable thermal drift and large crosstalk. The fabrication materials of the switches determine the switching times. These normally lie in the 10ms to 10μs time range [20]. MEMS optical space switches, built in a manner similar to silicon integrated circuits, have the advantages of high quality and high-port-count optical switching [22]. The movable torsion mirrors in these devices are controlled to redirect the propagation direction of light in order to achieve the required switching functionality. MEMS optical switches are a promising new technology as these switches also have fast speed, low loss and low crosstalk while being compact in size and economically attractive [23-25]. Finally, bubble switches are another kind of switches based on the new photonic-switching technology [26]. These switches use the bubbles generated in the etched trenches to reflect optical signals appropriately as per the switching requirements. Like MEMS switches, bubble switches also provide good performance with large scale integration at potentially low costs [26]. Both MEMS and bubbles switches have been getting substantial attention recently as potentially new technologies for flexible, large scale, low cost switches providing good performance. In this paper, we concentrate on MEMS and present new architectures for using this to obtain rearrangeable, non-blocking optical switches.

Since MEMS switches are expected to be an important new technology for all optical networking, we provide some further details on this here. These switches are divided into two sub-categories [22]. These are 3D MEMS switches and 2D MEMS switches. In an 3D switch, the mirrors can rotate along two axes and can assume a variety of positions. While this technology provides superior scalability, it would be extremely complex to fabricate and control [32]. In contrast, 2D MEMS switches trade-off ease of scalability for a far simpler two-position mirror operation. The mirrors rotate along one axis, and their states are referred to as either *lying* or *standing*. In this paper, we will focus on the study of 2D MEMS switches and their architecture.

The currently reported architectures for 2D MEMS switches have mostly been designed in a crossbar topology as shown in Fig. 1 [23-25]. Although such an architecture is simple and strictly non-blocking in nature, a very large number of micro-mirrors will be required to fabricate a large-scale switch block, e.g., an $N \times N$ MEMS optical switch block would require N^2 micro-mirrors. On the other hand, the strictly non-blocking switching capability may sometimes not even be necessary. For example, to switch wavelengths in an OXC node where the session requests are known a priori, an optical switch with the rearrangeable non-blocking switching capability is actually enough to achieve the required switching functionality. Because of this requirement, we have also proposed in this paper a rearrangeable non-blocking architecture for 2D MEMS optical space switches. The number of micro-mirrors required in this new architecture would be $\frac{N(N+1)}{2}$ as opposed to the N^2 required in the conventional crossbar design. We have also developed the associated routing algorithm to control the related micro-mirrors in a way so that we can guarantee the new architecture to be rearrangeable non-blocking. The scope of this study is on designing the new rearrangeable non-blocking architecture for 2D MEMS optical switches; we have not addressed the related issues of actual switch fabrication and physical performance measurements of these proposed switches.

The rest of this paper is organized as follows. Section II describes the conventional 2D MEMS switch architecture. Section III presents a new rearrangeable non-blocking architecture for 2D MEMS space switches. The corresponding routing algorithm to control the micro-mirror is also developed in the same section. Section IV evaluates the optimality of the proposed architecture, and computes a lower bound on the required number of micro-mirrors to achieve the rearrangeable non-blocking functionality. Section V discusses some of the properties of the new architecture, and the conclusions appear in the last section.

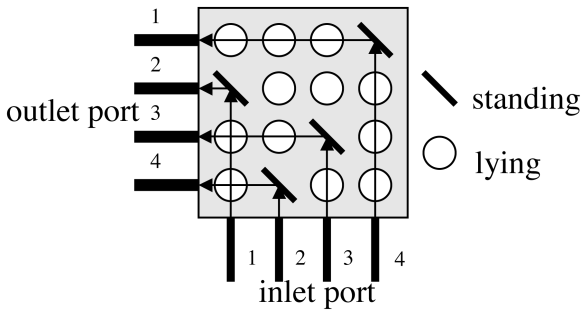

Figure 1: 4×4 strictly non-blocking conventional MEMS optical space switch.

2 Conventional 2D MEMS Space Switch Architecture

Fig. 1 typically illustrates a conventional 4×4 2D MEMS optical space switch. It consists of 4 inlet ports, 4 outlet ports and a total of 4×4 (=16) controllable micro-mirrors with single-face reflection. The switching functionality of such a block is achieved by controlling the state of those micro-mirrors. By making these mirrors *stand up* or *lie down,* the light from any inlet port can be switched to any desired outlet port [23-24]. For example, if the light from the inlet port 4 wants to switch to the outlet port 1, then the mirror at the position (1,4) is required to *stand up* to reflect the light; meanwhile, all the other micro-mirrors in the 1st row and the 4th column are set to *lie down* so as not to block the light that is passing through. This switch architecture is strictly non-blocking, that is, any connection can be established on demand in the switch block without affecting other existing connections. If both mirror faces are allowed to reflect light, then other architectures may also be proposed. Two architectures, which are specific to the situation that the connections are bi-directionally symmetric or the network nodal degree is 3, have been designed in [25], respectively. Although these two architectures are quite efficient in utilizing mirror faces (i.e., both mirror faces can reflect light), their serious limitation is that they require special traffic connections and network topologies, preventing them from being widely employed in general configurations.

3 Rearrangeable Non-Blocking Architecture for 2D MEMS Space Switches and the Routing Algorithm

Our proposed architecture for 2D MEMS space switches is given in Fig. 2, with various micro-mirrors controlled to be in the *standing* and *lying* states in order to give the arbitrary permutations shown. Both mirror faces in this architecture reflect light when it *stands up.* This new architecture requires only half of the total micro-mirrors required in the crossbar architecture. In addition, the new architecture belongs to a class of switches referred to as rearrangeable non-blocking. This implies that any possible permutation of the connections may be realised in this switch block by controlling the states of micro-mirrors; however, existing connections may have to be torn down and rearranged to route a new connection request. Showing that there exists a routing algorithm capable of configuring the micro-mirrors to achieve any arbitrary N to N permutation can prove the rearrangeable non-blocking nature of this 2D MEMS switch architecture.

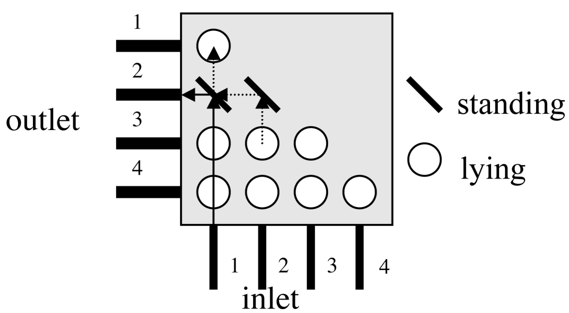

Figure 2: 4×4 rearrangeable non-blocking MEMS optical space switch with established connection from the inlet port 1 to the outlet port 2.

3.1 Notations

k: k^{th} inlet port, $k = 1,2,\ldots,N$.
O_k: the O_k^{th} outlet port corresponding to the k^{th} inlet port, that is, the light from the k^{th} inlet port is switched to the O_k^{th} outlet port, $k = 1,2,\ldots,N$.
S(j,k): the state of the micro-mirror at position *(j, k),* where j is the row index and k is the column index, $j = 1,2,\ldots,N$, $k \leq j$. $S(j,k) = 1$, if the micro-mirror at the position *(j,k)* is in the *standing* state; otherwise, $S(j,k) = 0$.
R(k): $k \rightarrow O_k^{th}$, $k = 1,2,\ldots,N$, which expresses the switching relationship between the inlet ports and the outlet ports, that is, the light from the k^{th} inlet port is switched to the O_k^{th} outlet port.
N: the number of inlet/outlet ports of a switch block, which corresponds to the switch dimension.

3.2 Routing/mirror control algorithm

(1) Initialisation: Set $S(j,k) = 0$, $j = 1,2,\ldots,N$, $k \leq j$. Initially, all the micro-mirrors are in the *lying state.*
(2) Route *R(1):* $1 \rightarrow O_1$ light by configuring the micro-mirror at the position $(O_1, 1)$ to *stand up,* i.e., $S(O_1, 1) = 1$. In Fig. 2, $O_1 = 2$.
(3) Also configure all the other micro-mirrors in the O_1^{th} row to *stand up,* i.e., set $S(O_1, j) = 1$, $1 < j \leq .O_1$. The aim of this is to guarantee that the light routed to those outlet ports, whose indexes are smaller than O_1, e.g. outlet port 1, reach their destinations through multiple reflections following the route of the dotted lines as illustrated in Fig. 2; otherwise, no light will be able to reach those outlet ports. For example in Fig. 2, if an inlet port whose index lies between 2 and 4 wants to reach outlet port 1, the light between them must be reflected by both the mirrors at the positions (2, 1) and (2, 2) along the route.
(4) Based on (3), we *virtually* remove all the mirrors on the O_1^{th} row and those on the 1st column which have row indexes larger than O_1, i.e. remove all the mirrors at the positions $\{(m,n)$: $m = O_1$, $1 \leq n \leq m\} \cup \{(m, n)$: $n = 1$, $m > O_1\}$. Now an $(N-1) \times (N-1)$ switch block is formed. For example in Fig. 2, all the mirrors on the 2nd row are removed, and all mirrors on the 1st column whose indexes are greater than 2 are also removed, then we can *virtually* form a 3×3 switch as shown in Fig. 3.

Note that the lights from the $(O_1 + 1)^{th}$ (e.g. 3rd in Fig. 2) row can always reach the $(O_1 - 1)^{th}$ (e.g. 1st in Fig. 2) row, because of the double reflections on the two neighbouring mirrors (e.g. on the 2nd column in Fig. 2) in step (3). It should also be noted that the *virtual removal* of mirrors from the

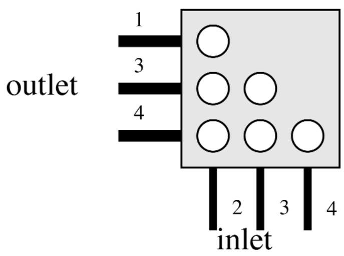

Figure 3: 3 × 3 rearrangeable non-blocking MEMS optical space switch after some mirrors are virtually removed.

O_1^{th} row with the condition that all these mirrors are standing up; however, the *virtual removal* of all the mirrors on the 1st column would leave all these mirrors lying down.

(5) Route the $(N - 1) \times (N - 1)$ block by recursively applying steps (1)-(4) and reducing the switch dimension by 1 on this iteration. Note that for this new $(N - 1) \times (N - 1)$ block, the mirror positions in the "new" first (input) column and the corresponding outlet row will be provided by steps (3) and (4) of the algorithm, as before.

(6) Repeat until the last (highest) inlet port is routed to its corresponding outlet port. Note that at the conclusion of this routing algorithm, the state of each of the $\frac{N(N+1)}{2}$ mirrors would be known so as to route each of the inlet ports to its corresponding outlet port.

As an example, Fig. 4(a)–(d) illustrates the processes that the routing algorithm is implemented for the session permutation $(1 \rightarrow 2, 2 \rightarrow 4, 3 \rightarrow 3, 4 \rightarrow 1)$.

3.3 Proving the proposed architecture to be rearrangeable non-blocking

According to the routing algorithm in Section 3.2, if an $(N-1) \times (N-1)$ MEMS switch block is rearrangeable non-blocking, an $N \times N$ switch block is also rearrangeable. The condition necessary to prove that the entire architecture for an arbitrary N is rearrangeable non-blocking is to prove the basic 2 × 2 switch block shown in Fig. 5 is rearrangeable non-blocking. By configuring the related micro-mirror states as shown in Fig. 5, the 2 × 2 switch block can obviously achieve the rearrangeable non-blocking functionality. (In fact, we can also verify that a 3 × 3 switch block is rearrangeable non-blocking by examining all of its six possible session permutations.) Thus, based on the above two conditions, we can claim that an arbitrary $N \times N$ MEMS space switch as shown in Fig. 2 will also be rearrangeable non-blocking in nature.

4 Optimality of the Proposed Architecture

It would be of interest to evaluate the optimality of our proposed architecture compared to others that might

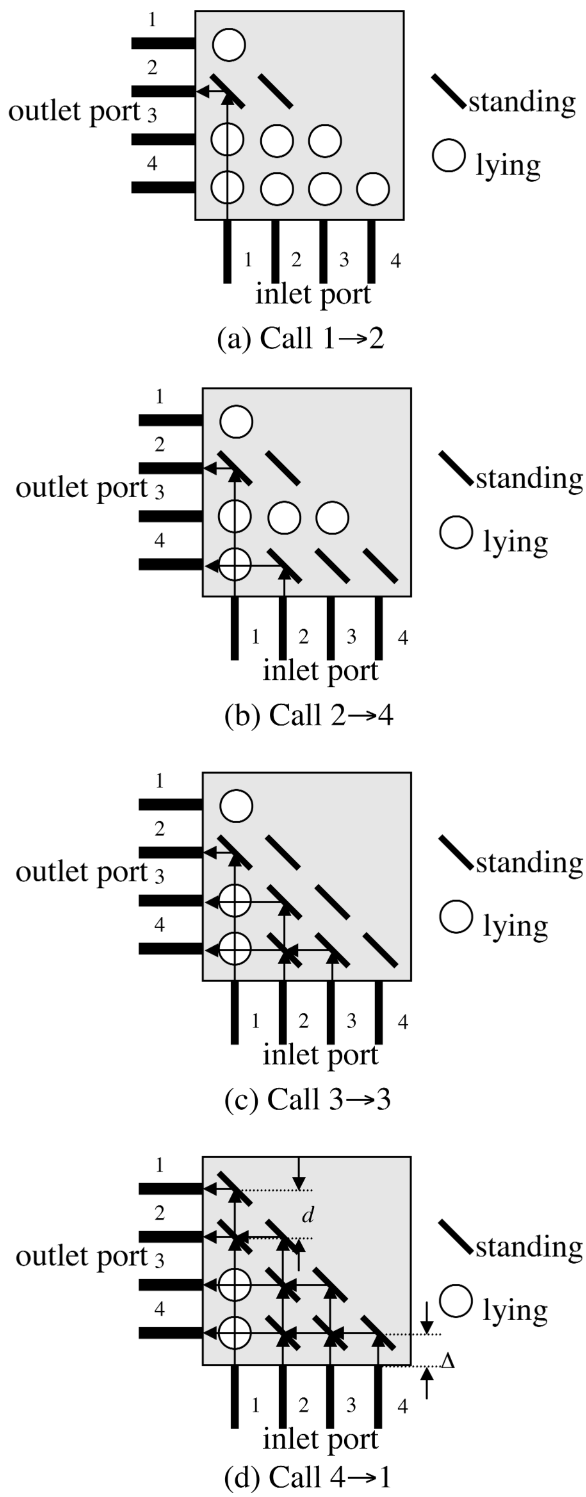

Figure 4: The process that the routing algorithm is implemented for the session permutation $(1 \rightarrow 2, 2 \rightarrow 4, 3 \rightarrow 3, 4 \rightarrow 1)$.

be used. The number of micro-mirrors is an important parameter for such comparisons. It can be shown that the number of cross-points in an $N \times N$ rearrangeable non-blocking electronic switching network would grow as $N \log_2 N$. Similarly, it has been shown in [30] that the required number of beta 2 × 2 optical waveguide switches

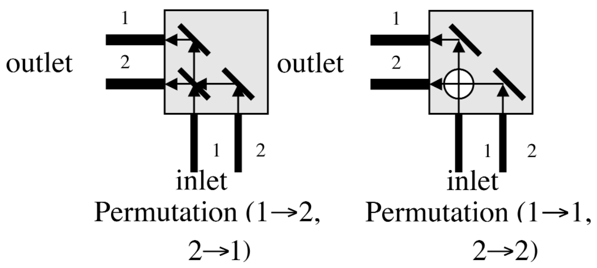

Figure 5: 2×2 rearrangeable non-blocking MEMS optical space switch.

in an $N \times N$ planar optical rearrangeable non-blocking switch block would be $N(N-1)/2$ or more. For the general 2D MEMS optical space switch, we show below that it is impossible to implement this with fewer than $N(N+1)/2$ micro-mirrors if we want to fabricate an $N \times N$ rearrangeable non-blocking switch block. Since our proposed MEMS switch needs only $N(N+1)/2$ micro-mirrors, we can conclude that our switch design is indeed optimal.

4.1 Lower bound on the number of micro-mirrors in a rearrangable, non-blocking 2D MEMS switch

To prove the $N(N+1)/2$ lower bound for a rearrangable non-blocking 2D MEMS switch, we use the same procedure as in [30]. Let m_N be the minimum number of micro-mirrors needed to fabricate an $N \times N$ rearrangeable non-blocking 2D MEMS optical space switch. For switching optical signals from N inlet ports to N outlet ports, there can be a total of $N!$ possible permutations. To discover the minimum required number of micro-mirrors, we must consider the worst cases. For even N, these occur when signals in the lower half of the inlet ports are to be mapped to the upper half of the outlet ports and vice versa. Since in this case all the $N/2$ connections from the lower half must cross all the $N/2$ connections from the upper half, this would require at least $N^2/4$ micro-mirrors. In addition, each half of the original inlet/outlets (of size $N/2$) may now be permuted among themselves, which would then need at least $2m_{N/2}$ micro-mirrors. Thus, when N is even,

$$m_N \geq \frac{N^2}{4} + 2m_{N/2} \quad (1)$$

For N odd, a similar argument, including two groups, one of $\lfloor N/2 \rfloor$ and the other of $\lfloor N/2 \rfloor + 1$, may be used to show that -

$$m_N \geq \lfloor N/2 \rfloor(\lfloor N/2 \rfloor + 1) + m_{\lfloor N/2 \rfloor} + m_{\lfloor N/2 \rfloor + 1} \quad (2)$$

Direct computations using (1) and (2) may be used to show that $m_N \geq \binom{N}{2} + N$ for $N = 2, 3,$ and 4. If we now assume that that $m_k \geq \binom{k}{2} + k = \frac{k(k+1)}{2}$ does hold for $k = 2,3,\ldots,N-1$, then we can show by induction that $m_N \geq \binom{N}{2} + N = \frac{N(N+1)}{2}$ also holds. For this, for even N, using (1), we have

$$m_N \geq N^2/4 + 2m_{N/2} \geq N^2/4 + 2\binom{N/2}{2} + N \geq \frac{N(N-1)}{2} + N = \binom{N}{2} + N,$$

and for odd N, using (2), we have

$$m_N \geq \lfloor N/2 \rfloor(\lfloor N/2 \rfloor + 1) + \binom{\lfloor N/2 \rfloor}{2} + \lfloor N/2 \rfloor + \binom{\lfloor N/2 \rfloor + 1}{2} + \lfloor N/2 \rfloor + 1 = \frac{N(N+1)}{2} = \binom{N}{2} + N$$

This proves that $m_N \geq \binom{N}{2} + N = \frac{N(N+1)}{2}$ as required for the general, rearrangable, non-blocking 2D MEMS switch. As mentioned earlier, since this is the number of mirrors required in our proposed architecture, this also proves the optimality of our proposed architecture for such switches.

5 Some Issues of Concern

5.1 Power loss

Studies [31] have shown that MEMS optical space switches show good performances in terms of extinction ratios (>60dB), crosstalk (<−60dB) and in lower (negligible) polarization and wavelength dependent losses. The fiber-to-fiber insertion loss of a single MEMS switch block mainly consists of four parts, which include loss due to Gaussian-beam divergence, loss due to angular misalignment, loss due to air absorption, and mirror reflection loss [31]. Gaussian-beam divergence is the phenomenon of the optical beams diverging through free space due to the finite emitting beam aperture. This imposes fundamental limits on the optical coupling efficiency. Angular misalignment is caused by the difficulties in accurately controlling the angle of the reflection mirror. This also detrimentally affects the optical coupling efficiency. The effect of air absorption also results in some loss when an optical beam passes through free space. Finally, mirror reflection loss is a loss caused by the mirror absorption when the mirror is reflecting light. Amongst these four losses, the first three are related to the free-space distance between the inlet port and the outlet port; therefore, for simplicity, we use a generic term called *loss due to free-space distance* to approximately represent the three of them in a combined fashion. Obviously, with increasing free-space distance between an inlet port and an outlet port, the loss due to free space distance will also increase. Therefore, to simplify the notation, we may use the free-space distance between the inlet port and the outlet port as a measure term to represent the loss due to this distance.

Specifically, the loss due to the angular misalignment of the micro-mirrors in our proposed architecture may be very different from that of the crossbar architecture. In the latter, each connection experiences only one micro-mirror reflection while going from the inlet port to the outlet port. Therefore, if the angular precision of the micro-mirrors is controlled well, then this loss may be very small and can be neglected. However, in our proposed architecture, the number of mirror reflections on a connection will not be constant, but will vary between 1 and $2N - 1$. Fig. 6(a)–(b) illustrates the light reflections when two neighbouring mirrors are misaligned in the same direction and the opposite directions. We observe that in the former case the effects of the misalignments of the two mirrors counteract with each other and the inlet light and the outlet light stay parallel. However, in the latter case, a 4θ angle is caused between the inlet light and the outlet light, which means that the effects of the misalignments of the two mirrors accumulate. Therefore, if the mirrors on a connection are misaligned in a certain pattern, i.e., all the neighbouring mirrors on the connection are misaligned in the opposite directions, then the accumulated angular misalignment between the inlet light and the outlet light will become $2N\theta$ for the longest connection, and correspondingly, the loss due to this misalignment will accumulate to be much higher than that in the conventional architecture. However, this may be overly pessimistic as the misalignments will actually be in random directions and may, to some extent, cancel each other out (e.g., when all the mirrors on the connection are misaligned in the same direction, the accumulated angular misalignment will be minimum).

A call switched by a rearrangeable nonblocking MEMS switch block will experience the free-space distance (loss) between an inlet port and outlet port, multiple mirror reflections, and fiber connection loss. Therefore, the total loss of a switched call may be expressed as

$$L(k, O_k) = (k - 1 + N - O_k)d\alpha + 2\Delta\alpha + t(k, O_k)\kappa + 2c \qquad (3)$$

with the following notations-

d: the free-space distance between two neighbouring mirrors as shown in Fig. 4(d); these two mirrors can be at the positions (i,j) and (i + 1,j), where $1 \le i \le N - 1$, $1 \le j \le N$, or, (i,j) and (i,j + 1), where $1 \le i \le N$, $1 \le j \le N - 1$.

Δ: the free-space distance between an inlet (outlet) port and its neighbouring mirrors as shown in Fig. 4(d).

κ: the reflectivity of micro mirrors; we have assumed that all the micro mirrors on the switch block have the same reflectivity.

α: the loss coefficient due to the free-space distance.

c: the connection loss between a fiber and a MEMS switch, which is assumed to the same for all the connections.

$t(k,O_k)$: the total number of mirror reflections as a function of the inlet port index k and the outlet port index O_k.

According to the routing algorithm in Section III, calls are switched by the order of the inlet index; that is, the call with the inlet index 1 is switched first, followed by the call with the index 2. This continues until finally the call with the index N is switched. Therefore, for a call, its *switching state* (which consists of the route gone through by the light beam, the number of mirror reflections, and the positions of the reflecting mirrors) is decided by the *switching states* of the other calls, which are switched earlier and whose inlet port indexes are smaller than that of the current call. We find the detailed expression for the function $t(k,O_k)$ as follows.

Starting from the call with the inlet index 1, we can always establish a connection for it through a single mirror reflection on the switch block. Thus,

$$t(1,O_1) = 1 \qquad (4)$$

For the call with the inlet index 2, we have

$$t(2, O_2) = \begin{cases} 1 & O_2 > O_1 \\ 3 & O_2 < O_1 \end{cases} \qquad (5)$$

This equation can be explained following the two cases illustrated in Fig. 2.

(1) If the outlet index of the call with the inlet index 2 is greater than that of the call with the inlet index 1

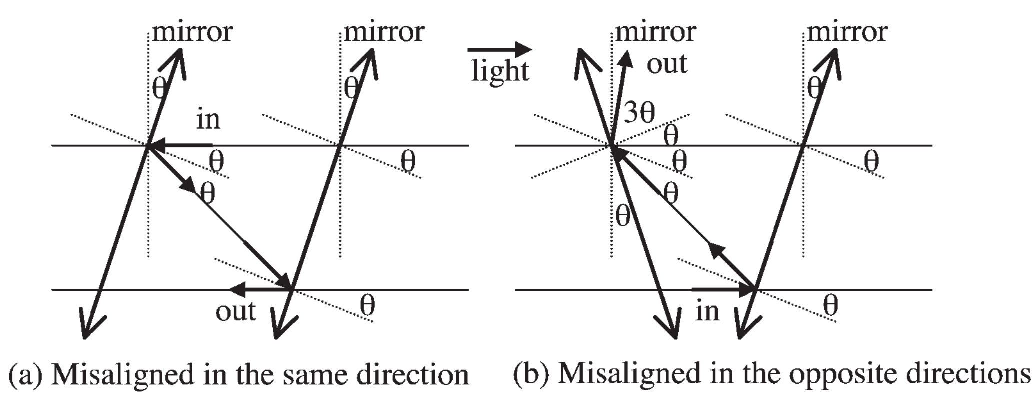

Figure 6: (a) Light reflection when neighbouring mirrors are misaligned in the same direction; (b) Light reflection when neighbouring mirrors are misaligned in the opposite directions.

(e.g., a call routed from inlet port 2 to outlet port 3 or 4), then this call does not need to experience the *double reflections* as shown on the 2nd row, as it can directly reach the outlet port with only a single mirror reflection.

(2) However, if the outlet index of the call with the inlet index 2 is smaller than that of the call with the inlet index 1 (e.g., a call routed from inlet port 2 to outlet port 1), then this call does need to experience the *double reflections* on the 2nd row before it goes to the outlet port. Therefore, the total number of mirror reflections in this case is 3.

In general case, for a call between the k^{th} inlet port and the O_k^{th} outlet port, we can have

$$t(k, O_k) = \begin{cases} 1 & O_k > \max(O_1, O_2, \ldots, O_{k-1}) \\ 2\sum_{l=1}^{k-1} \Phi(O_l, O_k) + 1 & otherwise \end{cases} \quad (6)$$

Here the function $\Phi(\bullet)$ is defined as $\Phi(p, q) = \begin{cases} 1 & p > q \\ 0 & p < q \end{cases}$. Similarly, the equation (6) can be explained for the following two cases.

(1) If the outlet port index O_k of the call is greater than all the outlet port indexes of the calls switched earlier, then the call can reach its outlet port with only one mirror reflection.

(2) However, if there are some switched calls whose outlet indexes are greater than that of the current call, then some *double reflections* are required before the light reaches the outlet port. The term $2\sum_{l=1}^{k-1} \Phi(O_l, Ok)$ is used to find the total number of mirror reflections due to the *double reflections.*

Based on the equation (6) and Fig. 2, we have the following theorem.

Theorem: Given a call $R(k)$: $k \rightarrow O_k$, $1 \leq k \leq N$, the minimum number of mirror reflections is equal to 1 when the condition $k \leq O_k$ is satisfied, and is equal to $2(k - O_k) + 1$ when the condition $k > O_k$ is satisfied; that is

$$\min_1 \{t(k, O_k)\} = \begin{cases} 1 & k \leq O_k \\ 2(k - O_k) + 1 & k > O_k \end{cases}, \quad (7)$$

and the maximum number of mirror reflections is equal to $2\min(k - 1, N - O_k) + 1$*; that is*

$$\max_1 \{t(k, O_k)\} = 2\min(k - 1, N - O_k) + 1 \quad (8)$$

Here the operations $\min_1$ and $\max_1$ are implemented among all the possible switched routes existing between the inlet port k and the outlet port O_k. The proof of the theorem is given in *Appendix A.*

Based on the above theorem, it is easy to find that for an $N \times N$ switch block, the minimum number of mirror reflections is 1 and the maximum number of mirror reflections is $2N - 1$ for the calls on the block. We can further find that the maximum number mirror reflection happens when a call is connected between the N^{th} inlet port and the 1^{st} outlet port, and in that case, $\min_1\{t(N,1)\} = \max_1 \{t(N,1)\} = 2N - 1$.

The reflectivity of a good gold-coated mirror is typically better than 97% (approximately 0.01dB) [31]. The average loss due to the free-space distance is in order of 0.1dB per pitch distance d (see Fig. 3 in [31]) for a switch block with the switch-mirror radius 150μm. Therefore, the loss due to mirror reflections is negligible compared to the loss due to free-space distance. In addition, given that the resolution of the mirror angular alignment can be further improved (so far, its state of art is in order of 0.1° [31]), the new proposed architecture is expected to have a scalability similar to that of the traditional crossbar architecture.

5.2 Two rearrangeable non-blocking switches on one substrate

For an $N \times N$ switch with the crossbar architecture, we would need a square substrate of size $(N - 1)d + 2\Delta$ with N^2 micro-mirrors. However, using our proposed architecture, we may accommodate two $N \times N$ rearrangeable non-blocking switches on the same square substrate as shown in Fig. 7. Therefore, the total required number of micro-mirrors of such two rearrangeable non-blocking is N^2, rather than $2\times(N(N + 1)/2) = N(N + 1)$ that may be expected. The reason of this is that these two rearrangeable non-blocking switches may share the micro-mirrors at the position $\{(m, n): m = n = 1,2,\ldots,N\}$, however, without degrading their independencies to achieve the switching functionalities. Additionally, the switch block as shown in Fig. 7 is flexible enough to work in two fashions. Basically, it can work as two $N \times N$ rearrangeable non-blocking switches. And in some situations, it may also work as an $N \times N$ strictly non-blocking switch if the functionality of strictly non-blocking is required.

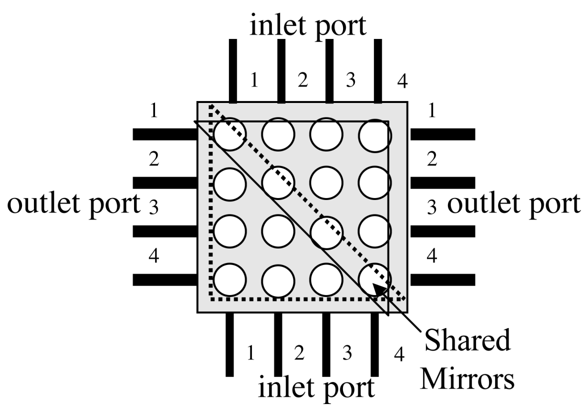

Figure 7: Two 4 × 4 rearrangeable non-blocking MEMS optical space switches on a single silicon substrate.

6 Conclusions

Optical switches are important components for all-optical networks. We have proposed a new rearrangeable non-blocking architecture for 2D MEMS optical space switches. The required number of micro-mirrors of the new design is found to be slightly more than half that of the conventional crossbar architecture. A simple routing/mirror control algorithm has also been given to guarantee the new architecture to be non-blocking in nature. To evaluate the optimality of the proposed architecture, we present a lower bound for the number of micro-mirrors in general rearrangeable non-blocking 2D MEMS space switches. Based on this we find that our proposed architecture is an optimal one.

7 References

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Appendix A:

Theorem: Given a call $R(k)$: $k \rightarrow O_k$, $1 \leq k \leq N$, the minimum number of mirror reflections is equal to 1 when the condition $k \leq O_k$ is satisfied, and is equal to $2(k - O_k) + 1$ when the condition $k > O_k$ is satisfied; that is

$$\min_1 \{t(k, O_k)\} = \begin{cases} 1 & k \leq O_k \\ 2(k - O_k) + 1 & k > O_k \end{cases}, \qquad (7)$$

and the maximum number of mirror reflections is equal to $2\min(k - 1, N - O_k) + 1$, *that is*

$$\max_1 \{t(k, O_k)\} = 2\min(k - 1, N - O_k) + 1 \qquad (8)$$

Proof: Based on (6), we can prove (7) as follows:
(i) For $k \leq O_k$, it is possible that all the outlet indexes from O_1 to O_{k-1} of the $k - 1$ switched calls are smaller than that of the current k^{th} call, (e.g., $O_i = i$, $i = 1,\ldots,k - 1$). Therefore, when $R \leq O_k$, $\min_1 \{t(k,O_k)\} = 1$.
(ii) For $k > O_k$, there are $k - 1$ calls switched before the k^{th} call, and for the outlet port O_k and there are at most $O_k - 1$ outlet ports whose indexes can be smaller than O_k. Thus, we find that there are at least $k - O_k$ calls whose outlet indexes are greater than O_k. This leads to

$$\min_1 \{t(k, O_k\} = 2(k - O_k) + 1.$$

Proving (7).
Based on (6), we can also prove the (8) as follows:
For a call $R(k)$: $k \rightarrow O_k$, there are at most $N - O_k$ outlet ports whose indexes are greater than O_k, and there are at most $k - 1$ calls switched before the k^{th} call, whose outlet port indexes are greater than O_k. Meanwhile, the constraint that a call corresponds to only a single outlet port should be satisfied. Therefore, the maximum number of the calls switched before the k^{th} call, whose outlet indexes are greater than O_k, is $\min\{N - O_k, k - 1\}$, which leads to

$$\max_1 \{t(k, O_k\} = 2\min \{k - 1, N - O_k\} + 1.$$

Proving (8).

Gangxiang Shen
Phone: 1 780 441 3856;
Fax: 1 780 441 3600;
Email: gshen@edm.trlabs.ca

Gangxiang Shen obtained his Bachelor Degree from the Department of Information and Electronics in Zhejiang University, P.R. China in 1997. He subsequently got his Master Degree (by research) from the School of Electrical and Electronic Engineering in Nanyang Technological University, Singapore in 1999. After that, he joined the laboratory of the Network Technology Research Center (NTRC) in the same university as a Research Associate. He is currently with Center for Optical Communication (COC) of Singapore as a Senior R&D Engineer. Mr. Shen's main research interests focus on all-optical networks. He is a member of IEEE. His home page may be found at http://hey.to/gxshen.

Dr. Tee Hiang Cheng

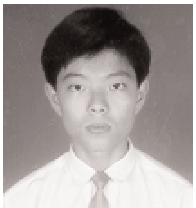
Dr. Tee Hiang Cheng received his B.Eng. and Ph.D. degrees from the University of Strathclyde in 1988 and 1992, respectively. He is an associate professor in the Communication Engineering Division of the School of Electrical and Electronic Engineering. He holds the concurrent appointment of Director of Network Technology Research Centre since 1998. He has been appointed, since 1994, by Infocomm Development Authority (IDA) to serve in its Telecommunication Standards Technical Committee (TSTC), which formulates telecommunication standards for Singapore. He is a member of the Management Committee of the $30m Singapore Advanced Research and Education Network (SingAREN) project jointly funded by the national Science and Technology Board (NSTB) and IDA. His main research interests include Asynchronous Transfer Mode Network and optical networking.

Chao Lu

Chao Lu received his B.Eng. degree in1985 from Tsing Hua University, Beijing, China, and M.Sc., Ph.D. degree from the University of Manchester Institute of Science and Technology (UMIST), U.K. in 1987 and 1990 respectively. He joined the School of Electrical and Electronic Engi-

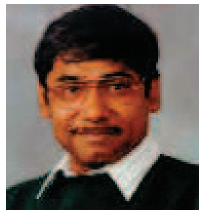
neering, Nanyang Technological University, Singapore, in 1991, where he is currently an associate professor in the communication division. His current research interests are in the area of optical communication systems and networks. In particular optical dense wavelength division multiplexing (DWDM) networks, fiber Bragg grating based WDM devices, optical subcarrier multiplexing systems and infrared wireless LANs.

Teck Yoong Chai



Teck Yoong Chai received the B.Eng. in electrical engineering from University of Malaya, Malaysia, in 1998, and completed his Ph.D. research at the Network Technology Research Centre, Nanyang Technological University, Singapore in 2001. He is currently with Kent Ridge Digital Labs. His field of interest is optical cross-connect system, in particular design and analysis of cross-connect switches.

Dr. Sanjay K. Bose
Phone: +91 512 597002
Fax: +91 512 590063
Email: skb@iitk.ernet.in



Dr. Sanjay K. Bose obtained his B.Tech. Degree from the Indian Institute of Technology, Kanpur in 1976 and was the President's Gold medallist of that year. He subsequently did his M.S. and Ph.D. from S.U.N.Y, Stony Brook, New York in 1977 and 1980, respectively. Dr. Bose was with the Communications Technology Program in the Corporate R & D Center of the General Electric Company at Schenctady during 1980-1982 and has been on the faculty of IIT, Kanpur since then. Dr. Bose has held visiting appointments at the University of Adelaide, Queensland University of Technology, Nanyang Technological University and several other universities. His research interests are in performance modeling, analysis and simulations of communication networks and queuing systems. He is a Senior Member of IEEE and is also member of Eta Kappa Nu and Sigma Xi. His home page may be found at http //home.iitk.ac.in/~skb.